REMARKS

Claims 1, 3-6, 8 and 10-12 are pending in this application. By this Amendment, claims 1 and 6 are amended, and claim 12 is added. No new matter is added. Claims 2, 7 and 9 are canceled without prejudice to or disclaimer of the subject matter recited in those claims. Reconsideration of the application based on the foregoing amendments and the following remarks is respectfully requested.

The Office Action rejects claim 6 under 35 U.S.C. §112, second paragraph, for being indefinite; rejects claims 1-11 under 35 U.S.C. §102(e) over U.S. Patent Application Publication No. 2004/0073773 to Demjanenko; rejects claims 1-11 under 35 U.S.C. §102(b) over U.S. Patent No. 6,189,094 to Hinds et al. ("Hinds"); and rejects claims 1-11 under 35 U.S.C. §102(b) over U.S. Patent No. 5,019,969 to Izumisawa et al. ("Izumisawa"). These rejections are respectfully traversed.

Claim 6 is amended to remove any ambiguity surrounding the term "predetermined element register." Accordingly, reconsideration and withdrawal of the rejection of claim 6 under 35 U.S.C. §112, second paragraph, are respectfully requested.

By this Amendment, the subject matter of claim 2 is included in independent claim 1. Claim 6 is also amended in like manner. Applicant asserts that, despite the rejection of claim 2 over each of Demjanenko, Hinds and Izumisawa, the subject matter of now canceled claim 2 as amended into claims 1 and 6 is not taught, nor would it have been suggested, by the applied prior art references.

The Office Action asserts that Demjanenko discloses a circuit for circularly specifying addresses of the vector register with the address of any element register of the vector register as the top (see first paragraph of page 3 of Office Action and Demjanenko paragraph [0668]). While Demjanenko does discuss a "circular buffer", Demjanenko does not suggest a register that is each of (i) a set of multiple scalar registers, (ii) in which any of the scalar registers may

be specified as the top register and (iii) the addresses of the multiple scalar registers are circularly specified, as recited in claim 1.

The Office Action further asserts that Hinds discloses a vector processor that includes a register with a set of multiple scalar registers, any of which may be designated as the top register, with the scalar register circularly specified (see paragraph 6 of the Office Action and col. 7, lines 36-67). However, while Hinds discloses vector operations in a sequence of registers in which the vector operations may "wrap" back to previous registers, Hinds does not disclose a vector processor in which any of the scalar registers can be specified as the top register and the addresses of the scalar registers are circularly specified. In fact, Hinds discloses, by way of example in Fig. 5, one vector processing operation in which the operation returns to the beginning of the sequence and repeats itself numerous times. Hinds does not disclose the use of a vector register in which the multiple scalar registers are circularly specified.

The Office Action further asserts that Izumisawa discloses a vector processor that includes multiple scalar registers, of which any scalar register can be specified as the top register, and the addresses of the multiple scalar registers are circularly specified (see paragraph 7 of the Office Action and col. 4, lines 42-49 of Izumisawa). However, Izumisawa actually discloses a system that uses two vector registers 100 and 101, and discloses a system where, rather than the vector registers being circularly specified, the system merely assigns the number "0" to the vector register after the number 63 is reached. Further, Izumisawa does not disclose a system in which any of the scalar registers can be specified as the top.

For at least the foregoing reasons, claims 1 and 6 recite features that are not disclosed by Demjanenko, Hinds or Izumisawa. Further, the claims depending from claim 1 are allowable for their dependence on claim 1, as well as for the additional features that they recite. Reconsideration and withdrawal of the rejection are respectfully requested.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1, 3-6, 8 and 10-12 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Daniel A. Tanner, III
Registration No. 54,734

JAO:PWO/gck

Date: July 19, 2006

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461